THE EFFECT OF ETCH FACTOR ON PRINTED WIRING CHARACTERISTIC IMPEDANCE

ABSTRACT

As logic switching speeds continue to increase, signal integrity becomes increasingly important. The signal paths have to be treated as transmission lines to accurately predict signal integrity. Many software tools exist to calculate transmission line characteristic impedance of printed-wiring traces as part of the overall signal analysis.

As the logic speeds get even faster, the effect of transmission line mismatch becomes more serious. Many of the software tools assume a rectangular cross-section for the traces. In actuality, the trace cross-sections more closely approximate a trapezoid due to the etching process.

We have used a field modeling program to determine the characteristic impedance of a variety of traces including buried microstrip, symmetrical stripline, edge-coupled pair, and broadside-coupled pair. These impedance determinations were performed with both rectangular and trapezoidal cross sections. In some cases, the difference in characteristic impedance between rectangular and trapezoidal cross-sections exceeded six percent.

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Introduction: The edge rate of digital signals on printed wiring boards continues to increase. For reliable operation we have to pay attention to *signal integrity*. For slow signals (edge rates) we could use *lumped* (or discrete) circuit analysis techniques to predict signal behavior. At faster edge rates we have to switch to *distributed* circuit analysis techniques to accurately predict signal behavior. This takes the form of *transmission line* analysis. We will quickly review the older lumped circuit analysis and see where it is no longer valid. A review of transmission lines will follow including a discussion of *characteristic impedance* and signal reflections. From there we will discuss *etch factor;* what it is and how it affects characteristic impedance. From there we will present the results of electromagnetic field simulations to determine the characteristic impedance of printed wiring traces with different etch factors.

Lumped Circuit Analysis: An example of a signal path suitable for lumped circuit analysis is shown in Figure 1.

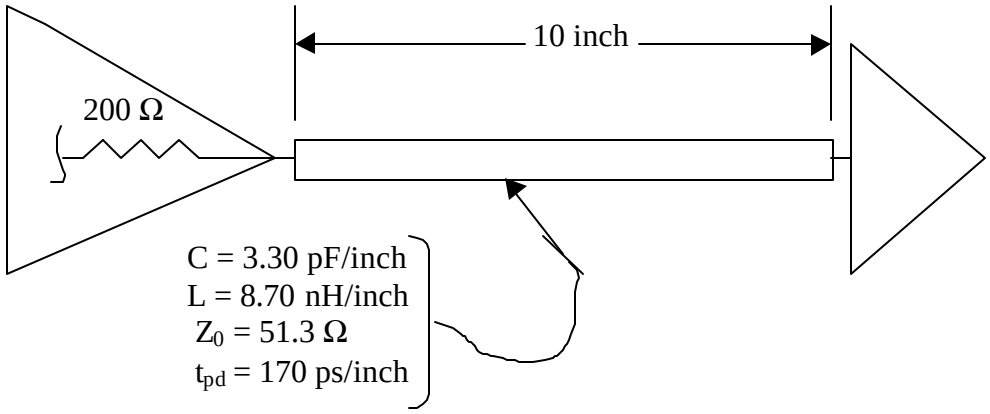


FIGURE 1: Digital Signal Path With Salient Parameters

Assuming really old technology, the output inherent rise time (i.e. unloaded output) of the driver is 12 ns. Note that the buffer propagation delay does not enter in here. It is only the rise time we are interested in.

The signal delay from the transmitter output to receiver input will be:
[path length (in inches)] [path delay (in ps/inch)] = [10 inch][170 ps/inch] = 1.7 ns.

Pages 7 and 8 of Reference 1 give a criteria for lumped versus transmission line analysis. *If the signal rise time is greater than six times the path delay, lumped analysis should suffice. If the signal rise time is less than six times the path delay, transmission line analysis is required.* In our example 12 ns > 6(1.7 ns) = 10.2 ns. Lumped analysis should be sufficient.

Assuming a high impedance receiver, we ignore the path inductance and concentrate on path capacitance: C_{path} = (10 inch)(3.3 pF/inch) = 33 pF. We will slightly simplify the analysis by ignoring the input capacitance of the receiver and the output capacitance of the driver.

The output driver 10 – 90 % rise time due to capacitive output loading is 2.2 RC time constants = 2.2(200 Ω)(33 pF) = 14.5 ns. The total output rise time can be approximated by the square root of the sum of the squares of the individual contributors. In this case:

$$T_{r\text{-}total} = \sqrt{T_{r1}^2 + T_{r2}^2} = \sqrt{(12\text{ ns})^2 + (14.5)^2} = 18.8\text{ ns}$$

We paid attention to C and t_{pd}, and ignored L and Z_0. Z_0 is the characteristic impedance of the transmission line and will be considered in the next section.

Transmission Line Basics: If we "soup up" the driver in Figure 1 by decreasing the output resistance to 20 Ω and assume an inherent rise time of 0.5 ns without external loading we will have to use transmission line analysis for valid analysis. Lets look first at transmission line basics and then apply it to the souped up driver. A typical transmission line for logic circuits is the *microstrip* shown in figure 2. It is a conductive trace in proximity to a signal return plane (ground or power).

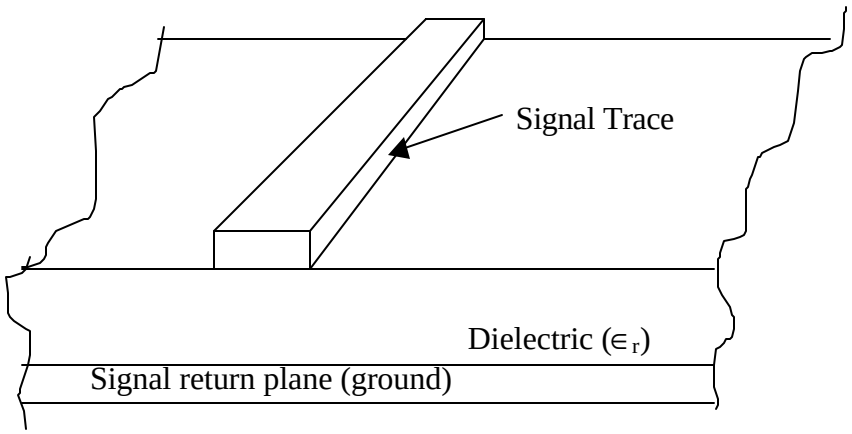


FIGURE 2: Microstrip Structure

The structure shown in Figure 2 is a surface microstrip. Had the signal trace been totally encased in dielectric it would be a buried microstrip. There are four stray effects to consider with this structure. There is resistance associated with the signal trace. The longer the trace, the greater the resistance. Likewise, there is inductance associated with the signal trace. The longer the trace, the greater the inductance. We can represent these two quantities as a series RL circuit. There is also capacitance from the signal trace to ground and a low conductance (high leakage) from trace to ground. Pulling this

altogether, we have the lossy transmission line equivalent circuit of Figure 3.

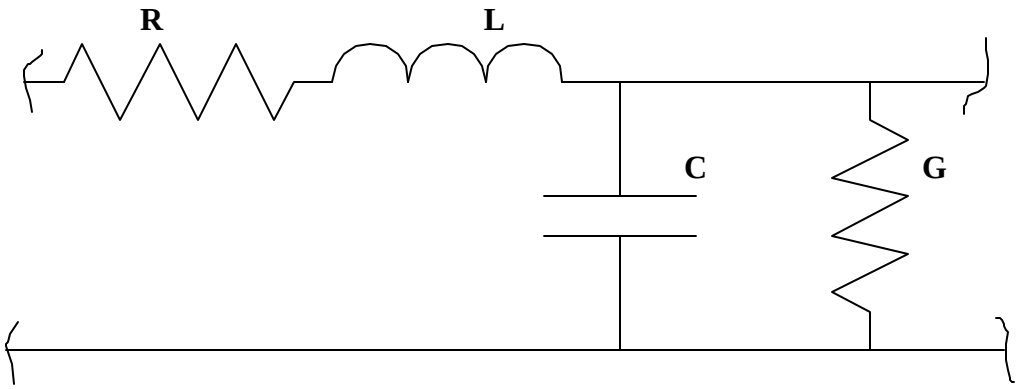


FIGURE 3: Lossy Transmission Line Section

Figure 3 depicts a distributed circuit (transmission line) as a lumped circuit equivalent. The accuracy of the model depends on how fine we make it. As an example, consider our ten inch trace from Figure 1. We could model that whole line with a single section with L = 87 nH and C = 33 pF. However, given a total section delay of 1.7 ns we can assume that the model is valid only for rise times greater than **(6)**(1.7 ns) or 10.2 ns. If we want the model to be accurate for 0.5 ns rise times, each section should have a delay less than (0.5 ns)/**6** = 83.3 ps. This implies we should have a minimum of : (1.7 ns)/(83.3 ps/section) = 20.4 sections. Rounding up to 21 sections we would model the line as a cascade of 21 identical sections. Each section would have L = (87 nH)/21 = 4.14 nH and C = (3.3 pF)/21 = 0.157 pF. The delay per section is then (1700 ps)/21 = 81.0 ps. In like manner, the total resistance of the line would be divided by 21 to get an equivalent R per section as would the total G also be divided by 21.

We can consider the line section to have a series impedance $Z = R + j\omega L$ where ω is (2π)(operating frequency). In like manner, the line section also has a shunt admittance $Y = G + j\omega C$. The characteristic impedance is given by: $Z_0 = (Z/Y)^{1/2}$. A discussion of characteristic impedance will follow shortly.

For most transmission lines; the capacitance is relatively constant with frequency, R above a certain frequency tends to increase as the square root of frequency, G increases with frequency, and L will change somewhat from a low frequency value to a lower value inductance at higher frequencies. The L and R variation with frequency is due to skin effect. More discussion on L and R can be found in Reference 2.

In many applications, the transmission line losses are relatively low which allows us to simplify the circuit of Figure 3. Generally, G does not affect us much until we are in the GHz range. Also, in many cases R is low enough that we can neglect it. This leaves a simpler transmission line section consisting only of L and C. This is the *lossless line.* Some useful transmission line approximations for the lossless line can be found in the appendix.

The lossless line allows us an easy way to visualize characteristic impedance. Consider the infinite-lossless transmission line in Figure 4.

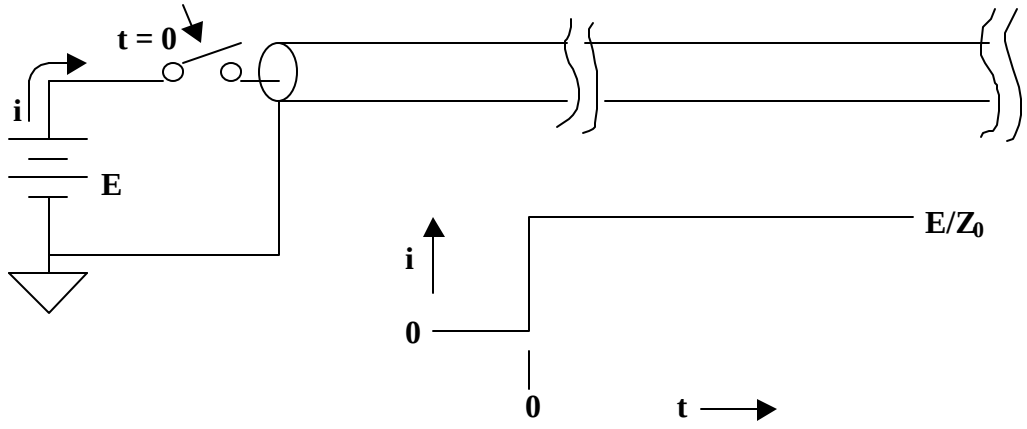


FIGURE 4: Infinite-Lossless Transmission Line

For the infinite-lossless line, the current remains constant with time. Each section charges up only to have the next section begin charging and drawing current. The current-voltage relationship appears to be that of a resistor. The characteristic impedance is the value of that apparent resistance. For the lossless line, the equation for characteristic impedance reduces to:

$$Z_0 = \sqrt{L/C}$$

Consider the transmission line in Figure 5 driving a load Z_L.

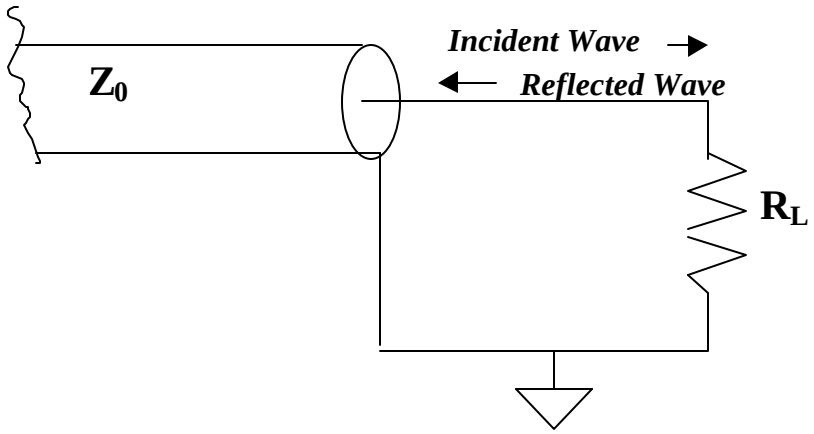


FIGURE 5: Transmission Line Driving a Load ($Z_L = R_L$)

In Figure 5 if $Z_0 = Z_L$, the *incident wave* that arrives at the end of the line is absorbed by the load and there is no reflection. If the load is not matched to the line, some of the energy will be reflected back as indicated by a *reflected wave.* The amount of reflection is given by:

$$\mathbf{r = \frac{Z_L - Z_0}{Z_L + Z_0}}$$ Where: ρ = the reflection coefficient ($-1.0 \le \rho \le +1.0$)

Z_0 = transmission line characteristic impedance

Z_L = load impedance

Example: If $Z_0 = 50\ \Omega$, $Z_L = 40\ \Omega$, and the incident wave is a 5 volt step:
$\rho = (40 - 50)/(40 + 50) = -0.1111$ which implies that 11.11 % of the incident wave is reflected back in the opposite polarity. (5V)(-0.1111) = -0.5555 volt reflected ⇒ we will have a net signal of 5 V – 0.5555 V = 4.4445 V at time of reflection.

Example: If $Z_0 = 50\ \Omega$, $Z_L = 60\ \Omega$, and the incident wave is a 5 volt step:
$\rho = (60 - 50)/(60 + 50) = +0.0909$ which implies that 9.09 % of the incident wave is reflected back in the same polarity. (5V)(0.0909) = +0.4545 volt reflected ⇒ we will have a net signal of 5 V + 0.4545 V at time of reflection.

For gross estimates we can approximate the reflection coefficient as being half the mismatch:

Z_L/Z_0	Mismatch	Mismatch/2	ρ
1.2	0.2	0.1	0.0909
0.8	- 0.2	- 0.1	- 0.1111
1.05	0.05	0.025	0.0243
0.95	- 0.05	- 0.025	- 0.0256

Referring to Figure 2 and taking on one other piece of information, we can get a good feel for what happens when we change the physical dimensions of the signal trace. For a given dielectric constant, the *propagation velocity* (v_p) of a lossless line is independent of the conductor dimensions. For a buried microstrip with thick dielectric, the *effective dielectric constant* ($\in_{r\text{-eff}}$) is equal to the material dielectric constant ($\in_r$). For a surface microstrip as shown in Figure 2, $\in_{r\text{-eff}} < \in_r$. In either case, the propagation velocity is given by:

$$\mathbf{v_p = \frac{c}{\sqrt{\in_{r\text{-eff}}}}}$$ Where c = speed of light in vacuum

c = 299,792,458 m/s ≈ 11.80 inch/ns

Propagation delay is the reciprocal of propagation velocity. In vacuum, propagation delay is 84.723 ps/inch. Thus, in general $t_{pd} = (84.723 \text{ ps/inch})(\in_{r\text{-eff}})^{1/2}$.

The propagation delay may also be found if L and C are known: $\mathbf{t_{pd} = \sqrt{LC}}$. Intuitively, we know the direction C will take for dimensional changes even though we may not know the amount. Whatever amount C changes, L will have to change by the same amount in the opposite direction in order to keep t_{pd} constant. Thus we can create the table on the next page with W = conductor width, H = conductor height above the ground plane, and T = conductor thickness. An upward arrow signifies an increase, a downward arrow signifies a decrease, and a dash signifies no change. It should be noted that this table is for high frequencies or the lossless case.

W	H	T	C	L	$Z_0 = (L/C)^{1/2}$
↑	—	—	↑	↓	↓
—	↑	—	↓	↑	↑
—	—	↑	↑	↓	↓

While we were able to qualitatively figure out the electrical effect of dimensional changes in the microstrip, getting quantitative results is much more difficult. Looking at the electric field of the microstrip as shown in Figure 6 gives us a hint as to why this is so.

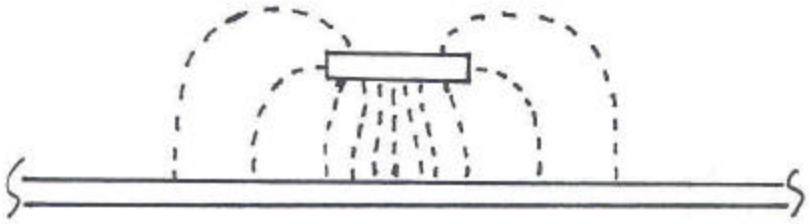


FIGURE 6: Microstrip Electric Field

Figure 6 is not quite accurate due to artistic limitations of the author. The fields entering and leaving a conductor should be perpendicular to the conductor. The purpose of the diagram is to illustrate the extent of stray fields which eliminates the use of the simple parallel plate capacitance equation. A great deal of work has been expended and continues to be expended to evaluate characteristic impedance. Reference 3 states that the only conductor configuration having an exact solution is coaxial cable. Many of the published solutions fail to give error bounds and range of applicability. One solution to the evaluation problem, particularly for unusual structures, is to use electromagnetic field solvers.

Transmission Line Analysis: Applying transmission line basics to the circuit of Figure 1 after it has been souped up by reducing the inherent driver rise time to 0.5 ns and reducing the output impedance to 20 Ω we begin by calculating the initial voltage at the input to the transmission line. We will assume that the unloaded output driver swings from 0 to 3.3 volts. The calculation is shown in Figure 7.

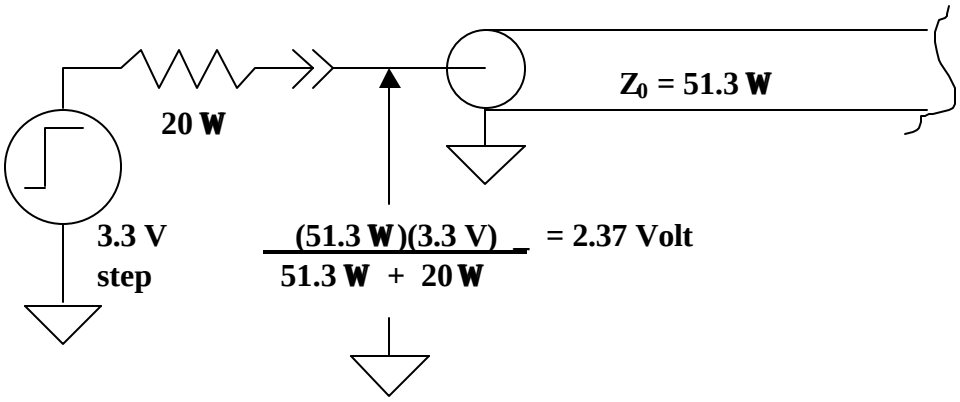


FIGURE 7: Calculation of Initial Driver Output Voltage

From Figure 7 we see that an incident 2.37 volt wave has been set in motion down the transmission line. One path delay (1.7 ns) later this incident waveform reaches the high-input-impedance receiver. This high impedance results in a reflection coefficient of ≈ +1. In essence, the 2.37 doubles to 4.74 volts when it hits the open-circuit receiver input. In a real logic circuit, diode clamps would limit this to something less than 4.74 volts but the purpose here is to apply and illustrate transmission line basics without undue complexity.

In another 1.7 ns, the 2.37 volt signal reflected from the receiver will arrive back at the transmitter. The transmission line will have a signal of 4.74 volts just prior to arriving at the transmitter. The reflection coefficient at this juncture is [(20 – 51.3)/(20 + 51.3)] = - 0.439. Thus the incident wave (2.37 V from receiver reflection) will be reflected back to the receiver with an amplitude of (-0.439)(2.37 V) = - 1.04 V. Thus at the driver, the voltage will now be 4.74 – 1.04 = 3.70 V. This back and forth reflection will continue for some time resulting in ringing.

There are many methods use to reduce transmission line reflections and ringing. Many of them require matching impedances which implies accurate knowledge of transmission line impedance.

Etch Factor: Many calculations concerning printed circuits assume a rectangular cross-section. Due to the fabrication process, the rectangular cross-section is only an approximation. In some cases the approximation may not be all that good. This affects resistance and impedance values. When changing vendors, different cross-sections for the same artwork can result due to different processes. For critical designs this might be problematical. By itself, etch factor may not be enough to cause the *nominal* value of characteristic impedance out of range but the tails of the distribution can result in low product yield.

Etch factor is discussed in References 4 and 5. Consider a printed circuit trace being etched by the old immersion process as shown in Figure 8.

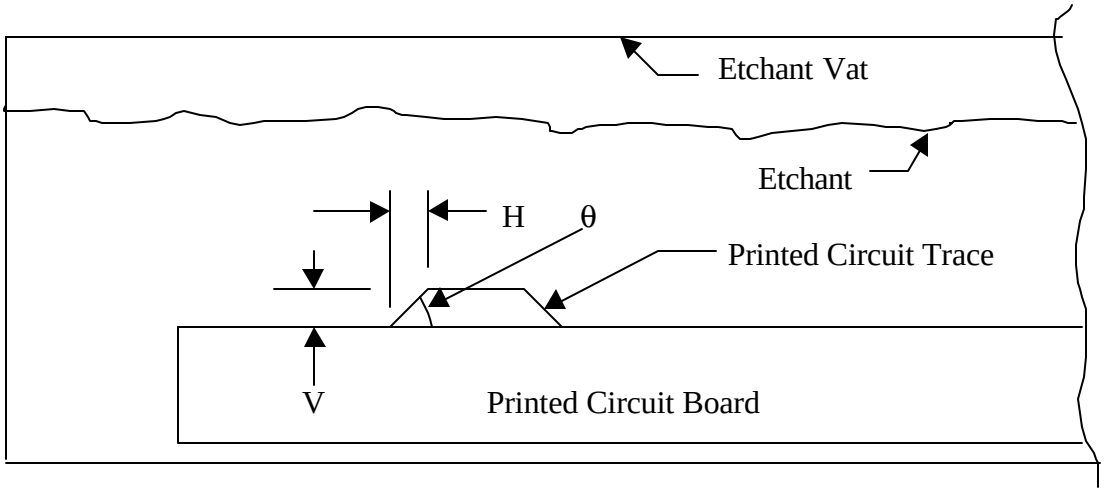


FIGURE 8: Immersion Etching Process

The etchant in Figure 8 not only dissolves copper in the vertical (V) direction, but it also dissolves copper in the horizontal (H) direction. Thus the formed trace will have a trapezoidal rather than triangular cross section. *Etch Factor* is defined as V/H. For the simple process shown the etch factor is one and the angle θ is arc tan (V/H) = 45°.

Improved etchants have been developed that etch further in the V direction than in the H direction. In addition, etchant spray processes have been developed to further enhance etching in the vertical direction. The net result is that etch factors in the three to eight range are available. When changing from one vendor (process) to another, there may be differences in the etch factor that will affect characteristic impedance. As the etch angle (θ) gets smaller, the electric field lines leaving the trace sides have a longer distance to travel resulting in a weaker field and hence smaller capacitance. Since the LC product remains constant, L must increase. The overall L/C ratio increases resulting in a higher characteristic impedance.

To evaluate the effect of etch factor on printed wiring impedance, several conductor configurations were evaluated with the Maxwell 2D electromagnetic field modeling software available from Ansoft. The first configuration evaluated was buried microstrip shown in Figure 9. Sometimes a *rectangular correction* is made. The idea is to take the area of the etched trapezoid and create a rectangle having the same area. This is ok for d.c. resistance calculations but is less effective for a.c. calculations. The rectangular equivalent is made by placing a midpoint on the sloping sides and then rotating these sides until a rectangle is formed. During the rotation, the thickness is not increased. An effective dielectric constant of 4.0 is used in the simulations.

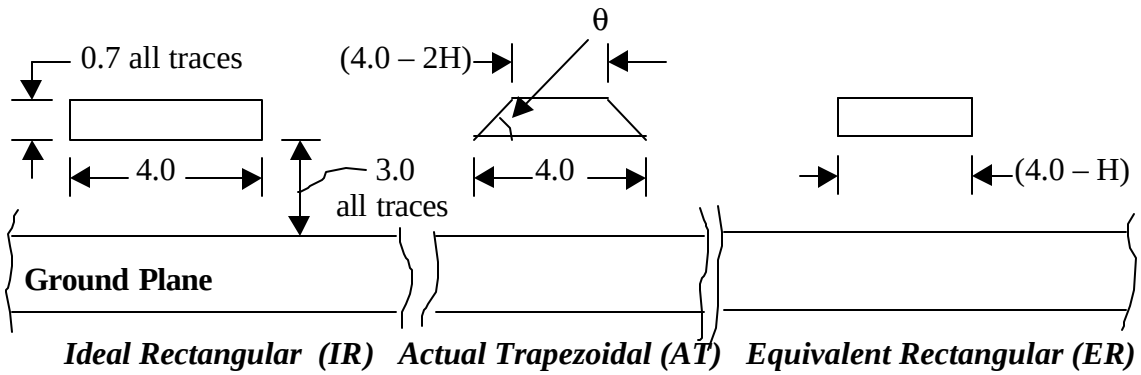


FIGURE 9: Buried Microstrip For Simulation, all dimensions in mils.

The Ansoft simulation data is shown in Tables 1 and 2.

TABLE 1: Buried Microstrip Simulation: Ideal Rectangular and Actual Trapezoidal

Etch Factor	Theta (deg)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (IR/AT)
Infinite	90.0	8.4833	3.3957	49.982	*N/A*
1.000	45.0	8.8440	3.2467	52.192	-4.23
1.732	60.0	8.7302	3.2890	51.521	-2.99
2.000	63.4	8.7031	3.2992	51.361	-2.68
3.000	71.6	8.6405	3.3231	50.991	-1.98
5.000	78.7	8.5873	3.3437	50.677	-1.37
8.000	82.9	8.5474	3.3593	50.442	-0.91

The infinite etch factor entry (Theta = 90.0) represents the ideal rectangular trace. The lower the etch factor, the further from the ideal rectangular trace. The lower etch factors result in lower capacitance since there is less fringe field from trace to ground. For t_{pd} to remain constant; if C decreases with lower etch factor, then L must increase since $t_{pd} = (LC)^{1/2}$. The propagation delay (t_{pd}) is also equal to ($t_{pd\text{-}vacuum}$)($\in_r$). Since the effective relative dielectric constant for this configuration does not change with etch factor, the LC product must be constant. It should be noted that all the simulation values are high frequency values. We have not considered dispersion at low frequencies. For high speed digital signaling, this is a reasonable approach.

The **%D (IR/AT)** entry is the percentage deviation of the characteristic impedance (Z_0) of the ideal rectangular cross section (etch factor = infinity) with respect to the actual trapezoidal cross section.

Figures 10 and 11 are plots of the buried microstrip parameters versus etch factor.

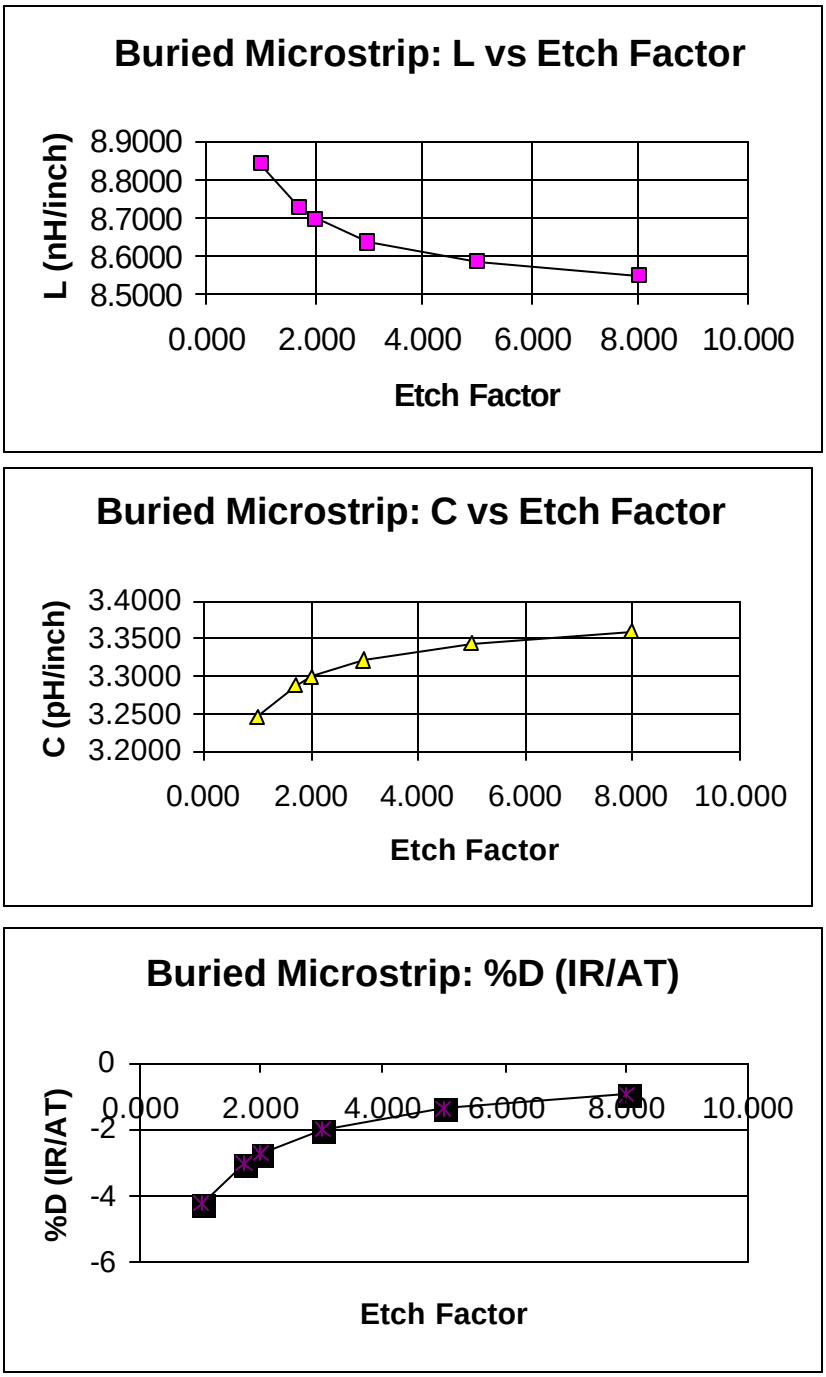


FIGURE 10: Buried Microstrip Parameters as a Function of Etch Factor

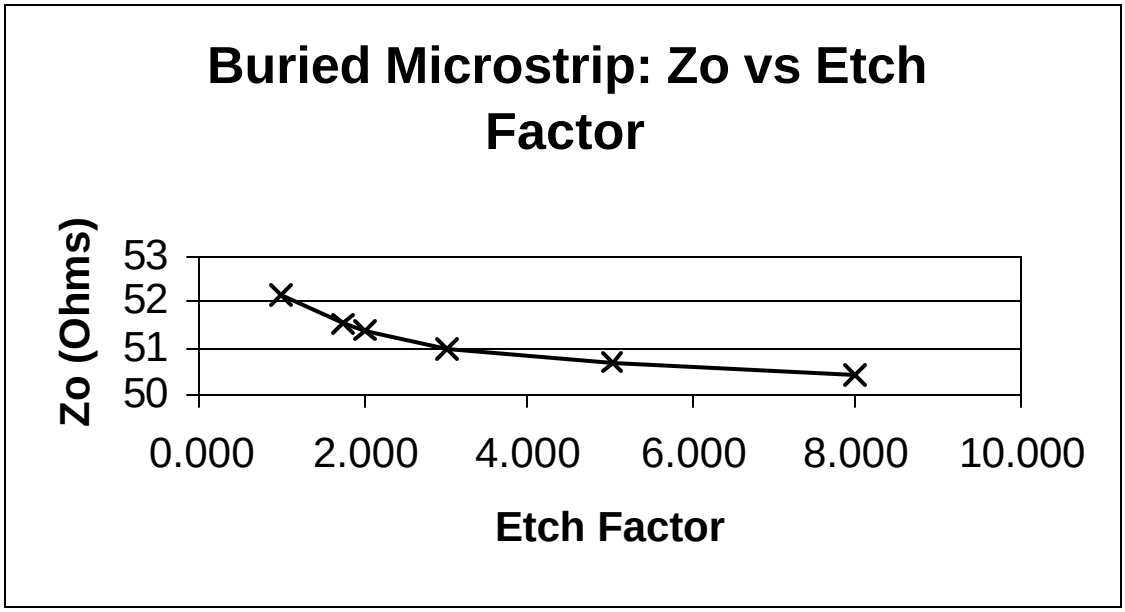


FIGURE 11: Buried Microstrip: Z_0 versus Etch Factor

The rectangular correction (equivalent rectangle) simulations for buried microstrip is tabulated in Table 2.

TABLE 2: Buried Microstrip Simulation: Equivalent Rectangular

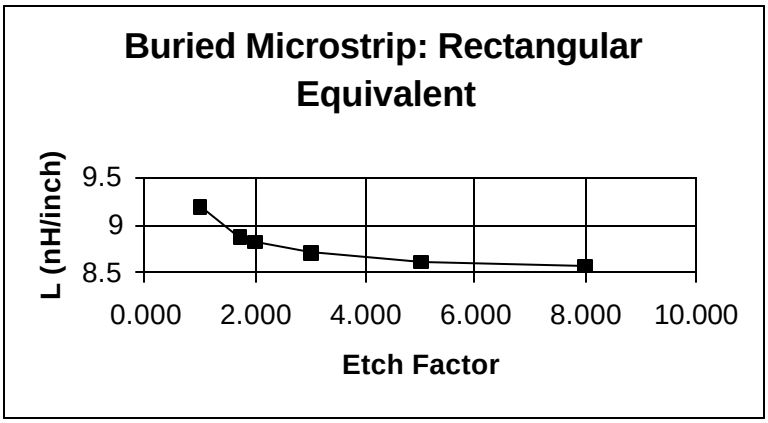
Etch Factor	w (mils)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (ER/AT)
1.000	3.30	9.1879	3.1252	54.222	3.89
1.732	3.60	8.8726	3.2362	52.361	1.63
2.000	3.65	8.8192	3.2677	51.951	1.15
3.000	3.77	8.7056	3.2983	51.375	0.75
5.000	3.86	8.6105	3.3347	50.814	0.27
8.000	3.91	8.5678	3.3513	50.562	0.24

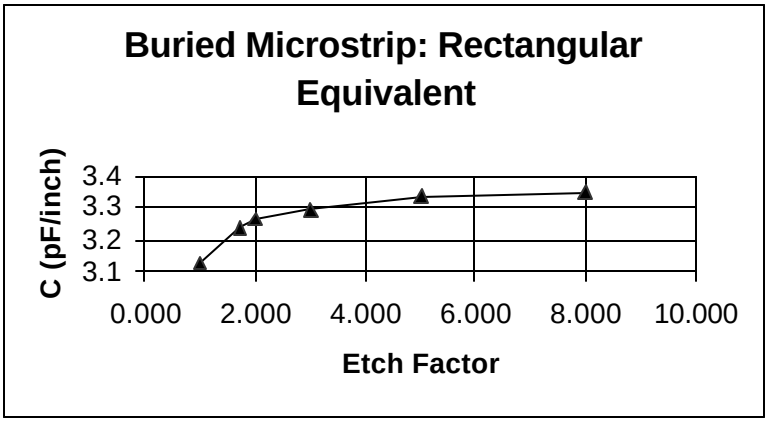
The width (w) of the equivalent rectangular trace is 4.0 mils – H where H = 0.7/(etch factor).

Comparing to Table 1, we see from Table 2 that: the equivalent rectangular L is higher for all etch factors than the actual trapezoidal and also that C is lower than the actual trapezoidal for all etch factors. The Z_0 of the equivalent rectangular is higher than Z_0 of the actual trapezoidal for all etch factors.

The **%D (ER/AT)** column is the percentage deviation of the equivalent rectangular Z_0 with respect to the actual trapezoidal Z_0. Note that the magnitude of these deviations are somewhat less than the %D (IR/AT) deviations but not by a whole lot (particularly at lower etch factors). Also note the change in sign.

Figures 12 and 13 are plots of the equivalent rectangular buried microstrip parameters as a function of etch factor.





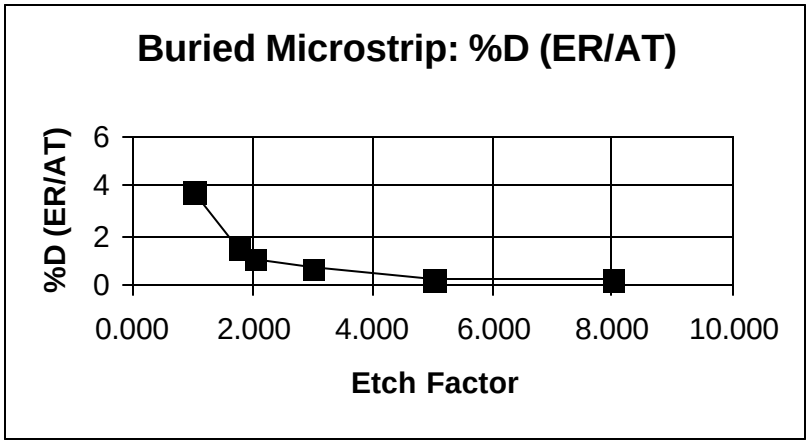


FIGURE 12: Equivalent Rectangular Buried Microstrip Parameters versus Etch Factor

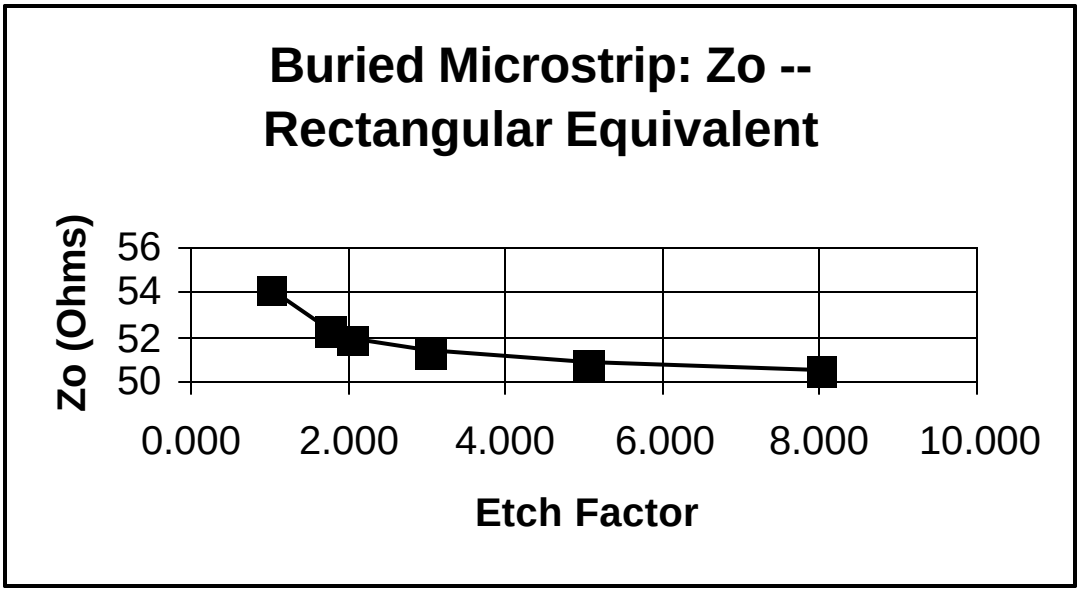
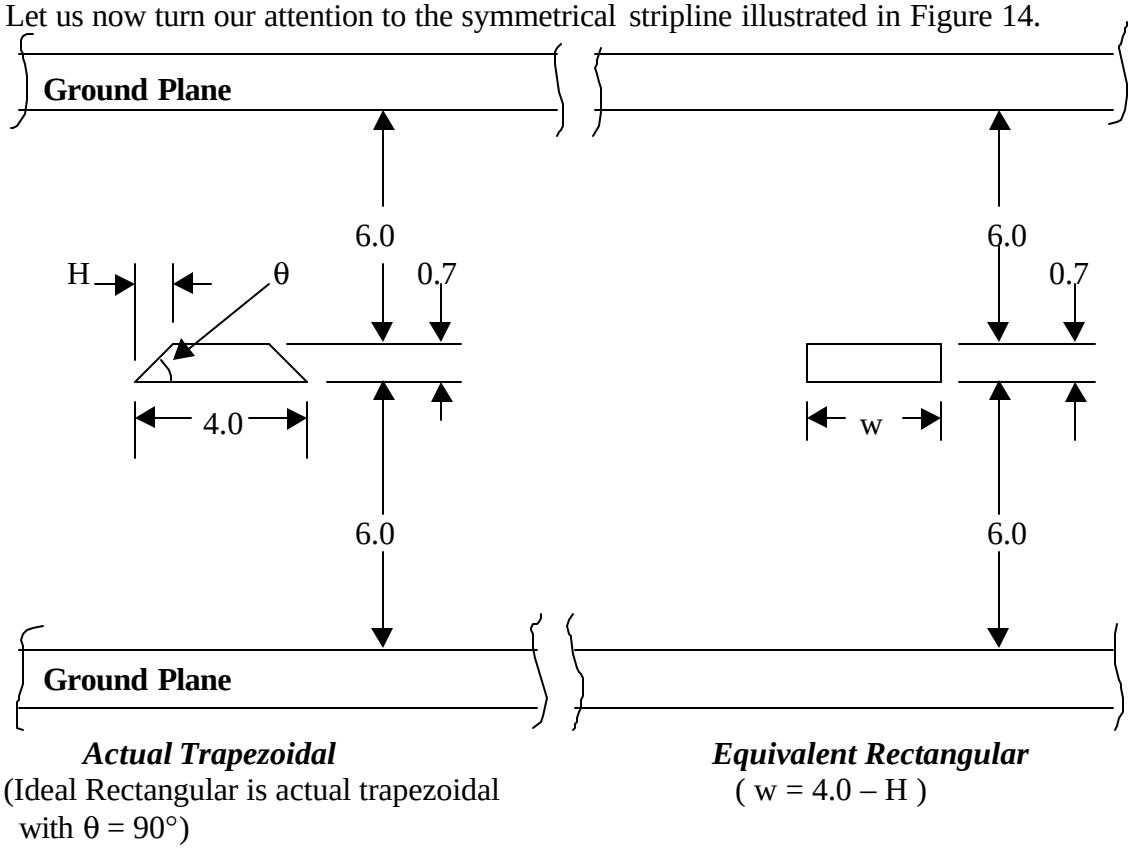


FIGURE 13: Equivalent Rectangular Buried Microstrip Z_0 versus Etch Factor

Let us now turn our attention to the symmetrical stripline illustrated in Figure 14.



Actual Trapezoidal
(Ideal Rectangular is actual trapezoidal with θ = 90°)

Equivalent Rectangular
(w = 4.0 – H)

FIGURE 14: Symmetrical Stripline for Simulation, all dimensions in mils.

In the stripline, return current flows through both ground/power planes. This is a very common structure in multilayer printed wiring boards although the spacing in that application tends to be asymmetrical (i.e. the signal conductor will be closer to one plane than the other). As with buried microstrip, we also looked at the equivalent rectangular cross section for the symmetrical stripline. Note that we doubled the spacing from signal to ground plane in an attempt to maintain an impedance similar to the microstrip. Keeping the same spacing would almost double the capacitance and if the capacitance doubled, the inductance would have to be reduced by half in order to maintain the same propagation velocity. The combined effect of capacitance and inductance changes would be to cut the characteristic impedance in half.

The tabular simulation data for symmetrical stripline are given in Tables 3 and 4. The *magnitude* of the impedance deviations is given in Figure 15.

TABLE 3: Symmetrical Stripline Simulation, Ideal Rectangular and Actual Trapezoidal

Etch Factor	Theta (deg)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (IR/AT)
Infinite	90.0	9.3906	3.0639	55.361	*N/A*
1.000	45.0	9.8652	2.9220	58.105	-4.72
1.732	60.0	9.7116	2.9662	57.220	-3.25
2.000	63.4	9.6743	2.9783	56.994	-2.87
3.000	71.6	9.5931	3.0049	56.502	-2.02
5.000	78.7	9.5147	3.0271	56.064	-1.25
8.000	82.9	9.4720	3.0393	55.826	-0.83

TABLE 4: Symmetrical Stripline Simulation, Equivalent Rectangular

Etch Factor	w (mils)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (ER/AT)
1	3.3	10.113	2.8423	59.649	2.66
1.732	3.6	9.7973	2.9395	57.732	0.89
2	3.65	9.7438	2.956	57.413	0.74
3	3.77	9.6173	2.9943	56.673	0.3
5	3.86	9.5251	3.0219	56.143	0.14
8	3.91	9.4755	3.0375	55.852	0.05

From Figure 15 we can see that for etch factors greater than 1.7, the equivalent rectangular approach results in less than 1% error for characteristic impedance. For these etch factors and if your available field modeling software does not allow trapezoidal cross sections, a rectangular equivalent model can afford a reasonable accuracy.

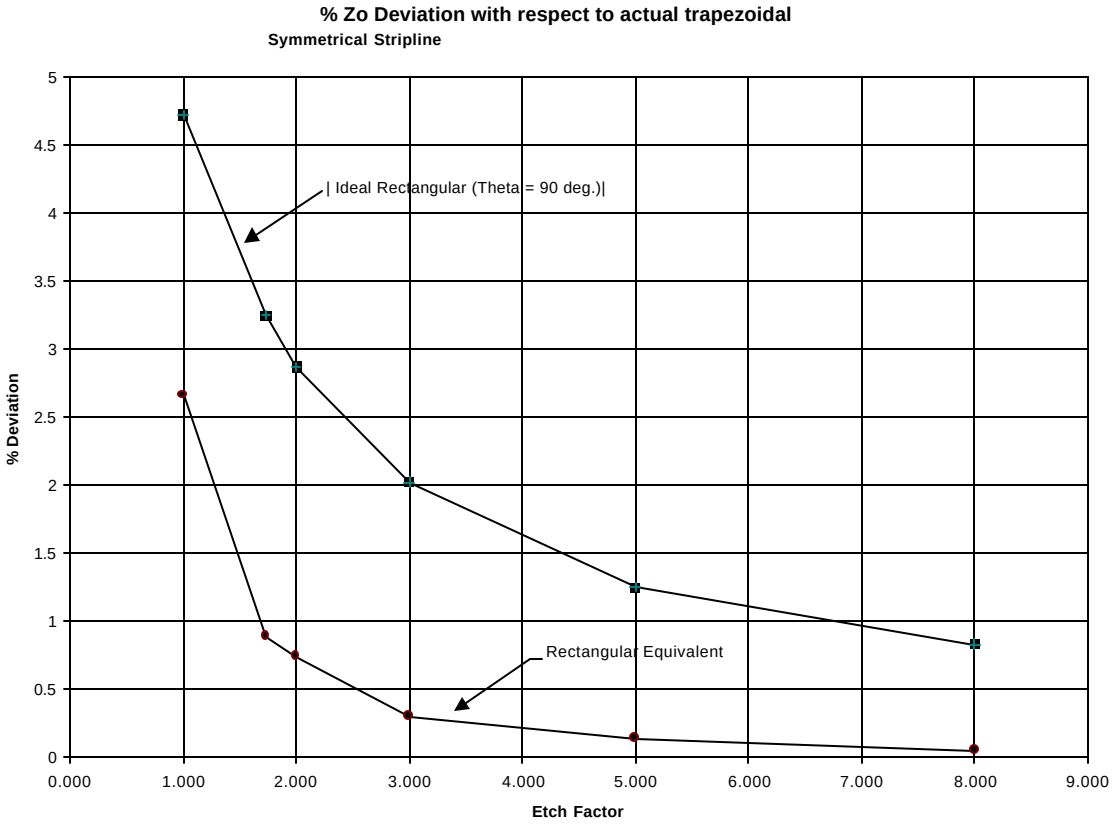


FIGURE 15: Characteristic Impedance Deviation With Respect to Actual Trapezoidal Cross Section, Symmetrical Stripline.

High speed digital signaling requirements have led to increased use of differential signal transmission. Two popular configurations for differential signal transmission are the edge-coupled pair and the broadside coupled pair.

Starting with the edge-coupled pair we looked at buried microstrip and surface microstrip. The buried microstrip version is illustrated in Figure 16 and simulation data is presented in Tables 5 and 6. The *magnitude* of the impedance deviations is plotted in Figure 17. Note the 6% error between ideal rectangular and actual trapezoidal for characteristic impedance.

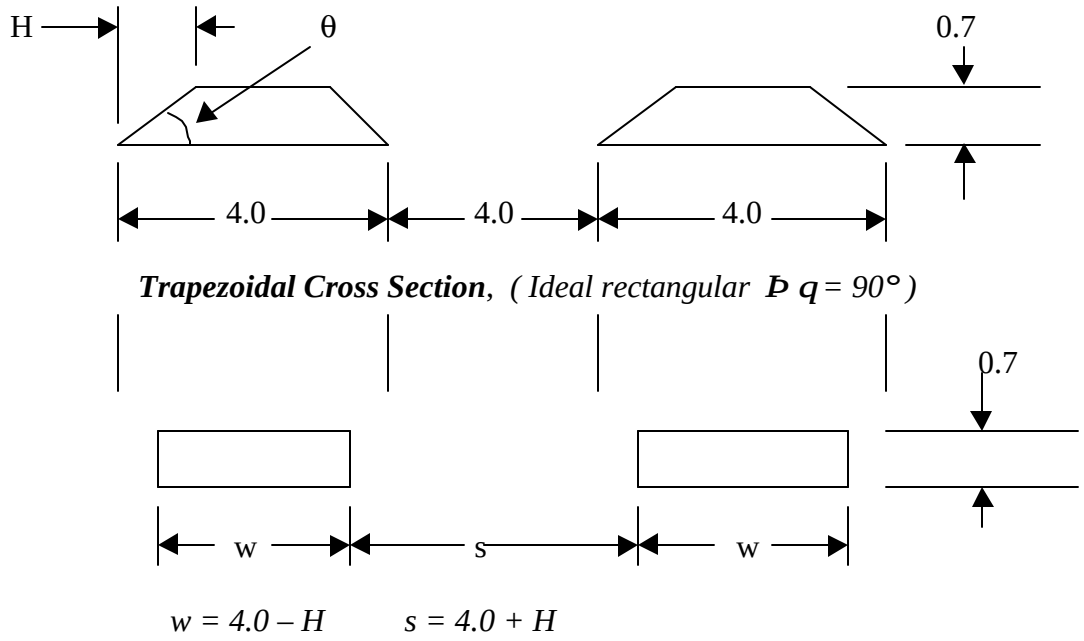


FIGURE 16: Edge-Coupled Pair, Buried Microstrip

TABLE 5: Edge-Coupled Pair, Buried Microstrip – Ideal Rectangular and Actual Trapezoidal

Etch Factor	Theta (deg)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (IR/AT)
Infinite	90.0	17.444	1.6460	102.95	*N/A*
1.000	45.0	18.595	1.5442	109.74	-6.19
1.732	60.0	18.230	1.5751	107.58	-4.30
2.000	63.4	18.173	1.5800	107.25	-4.01
3.000	71.6	17.958	1.5989	105.98	-2.86
5.000	78.7	17.757	1.6170	104.79	-1.76
8.000	82.9	17.642	1.6275	104.12	-1.12

TABLE 6: Edge-Coupled Pair, Buried Microstrip – Equivalent Rectangular

Etch Factor	w (mils)	s (mils)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	% D (ER/AT)
1.000	3.30	4.70	19.275	1.4897	113.75	3.65
1.732	3.60	4.40	18.463	1.5552	108.96	1.28
2.000	3.65	4.35	18.333	1.5663	108.19	1.55
3.000	3.77	4.23	18.047	1.5938	106.41	0.41
5.000	3.86	4.14	17.784	1.6146	104.95	0.15
8.000	3.91	4.09	17.659	1.6260	104.22	0.01

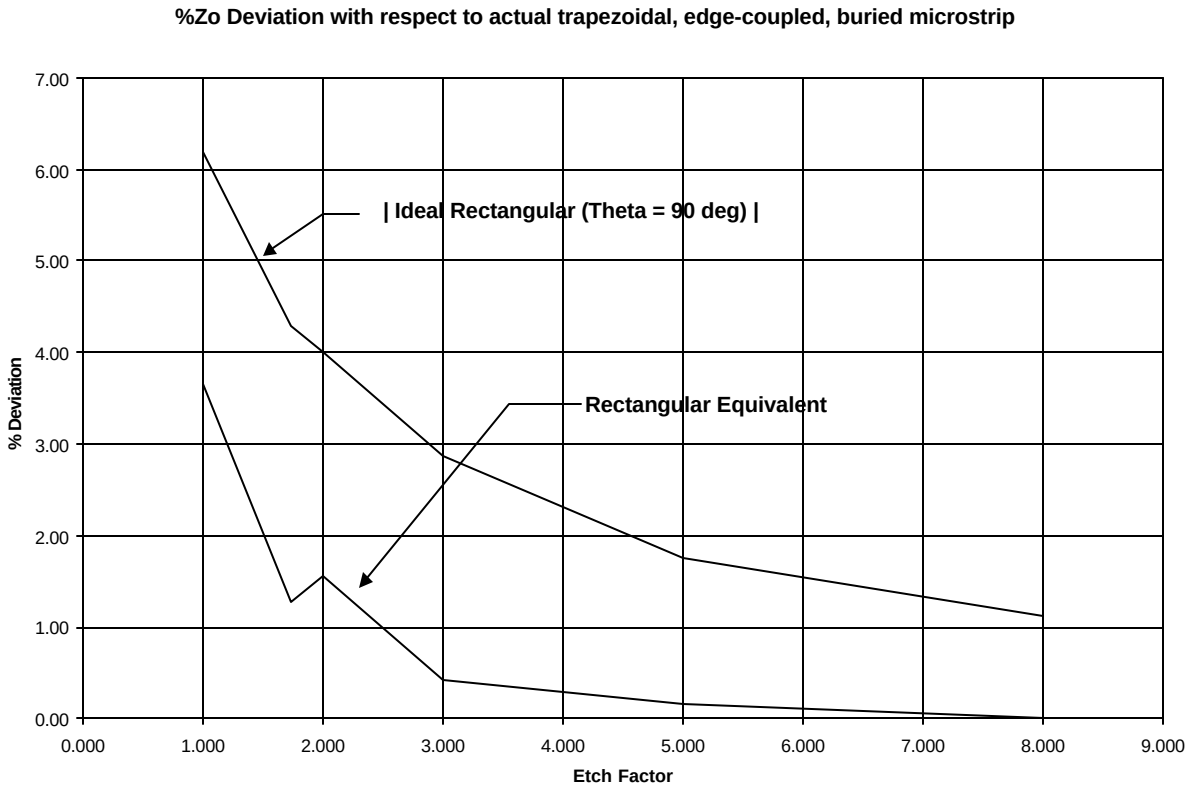


FIGURE 17: Characteristic Impedance Deviation With Respect to Actual Trapezoidal Cross Section, Edge-Coupled, Buried Microstrip

Surface microstrip is illustrated in Figure 18. The bottom of the traces are in contact with the dielectric material ($\in_r = 4.0$) but the rest of the traces are in air. The effect is to have an effective dielectric constant less than 4.0. In an actual printed wiring board this structure is likely to be somewhat modified with the addition of a thin layer of solder mask that will increase the effective dielectric constant somewhat.

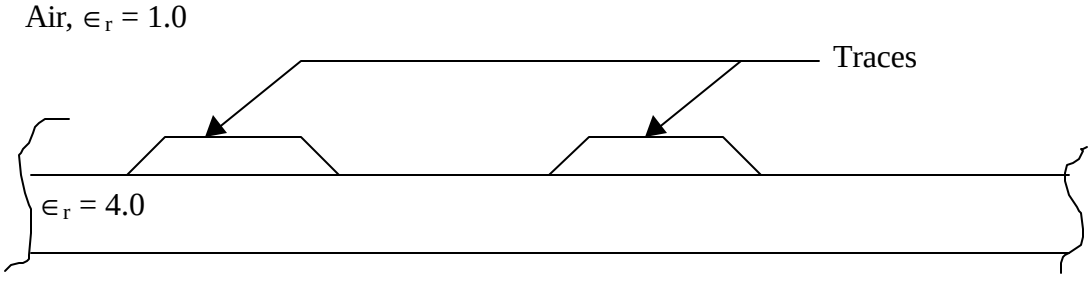


FIGURE 18: Surface Microstrip, Edge Coupled Pair

The transmission line parameters for the surface microstrip, edge-coupled pair are given in Tables 7 and 8. Notice that an additional column (Tpd) has been added. This is the propagation delay calculated on the basis of a lossless line. The percentage deviation of the characteristic impedance for ideal rectangular and equivalent rectangular with respect to actual trapezoidal is plotted in Figure 20. The propagation delay for the actual trapezoidal is plotted in Figure 19.

TABLE 7: Edge-Coupled Pair, *Surface Microstrip* – Ideal Rectangular and Actual Trapezoidal

Etch Factor	Theta (deg)	L (nH/inch)	C (pF/inch)	Tpd (ps/inch)	Zo (Ohms)	%D (IR/AT)
Infinite	90.0	17.453	0.92936	127.4	137.04	*N/A*
1.000	45.0	18.630	0.89642	129.2	144.17	-4.95
1.732	60.0	18.261	0.90517	128.6	142.04	-3.52
2.000	63.4	18.178	0.90702	128.4	141.57	-3.20
3.000	71.6	17.964	0.90990	127.8	140.51	-2.47
5.000	78.7	17.774	0.91604	127.6	139.29	-1.62
8.000	82.9	17.651	0.92080	127.5	138.45	-1.02

TABLE 8: Edge-Coupled Pair, *Surface Microstrip* – Equivalent Rectangular

Etch Factor	w/s (mils)	L (nH/inch)	C (pF/inch)	Tpd (ps/inch)	Zo (Ohms)	%D (ER/AT)
1.000	3.30/4.70	19.305	0.83928	127.3	151.67	5.20
1.732	3.60/4.40	18.498	0.87819	127.5	145.13	2.18
2.000	3.65/4.35	18.359	0.88319	127.3	144.18	1.84
3.000	3.77/4.23	18.052	0.89974	127.4	141.65	0.81
5.000	3.86/4.14	17.810	0.91097	127.4	139.83	0.39
8.000	3.91/4.09	17.683	0.91733	127.4	138.84	0.28

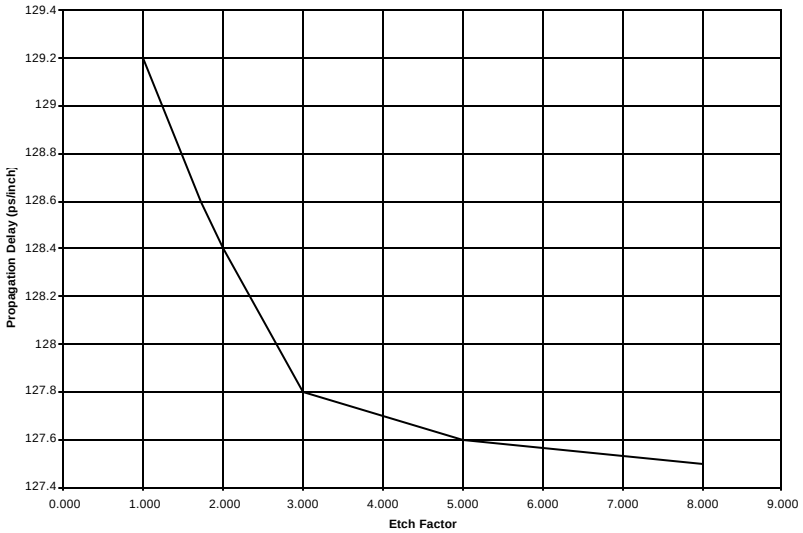


FIGURE 19: Propagation Delay vs Etch Factor; Surface Microstrip, Edge-Coupled Pair

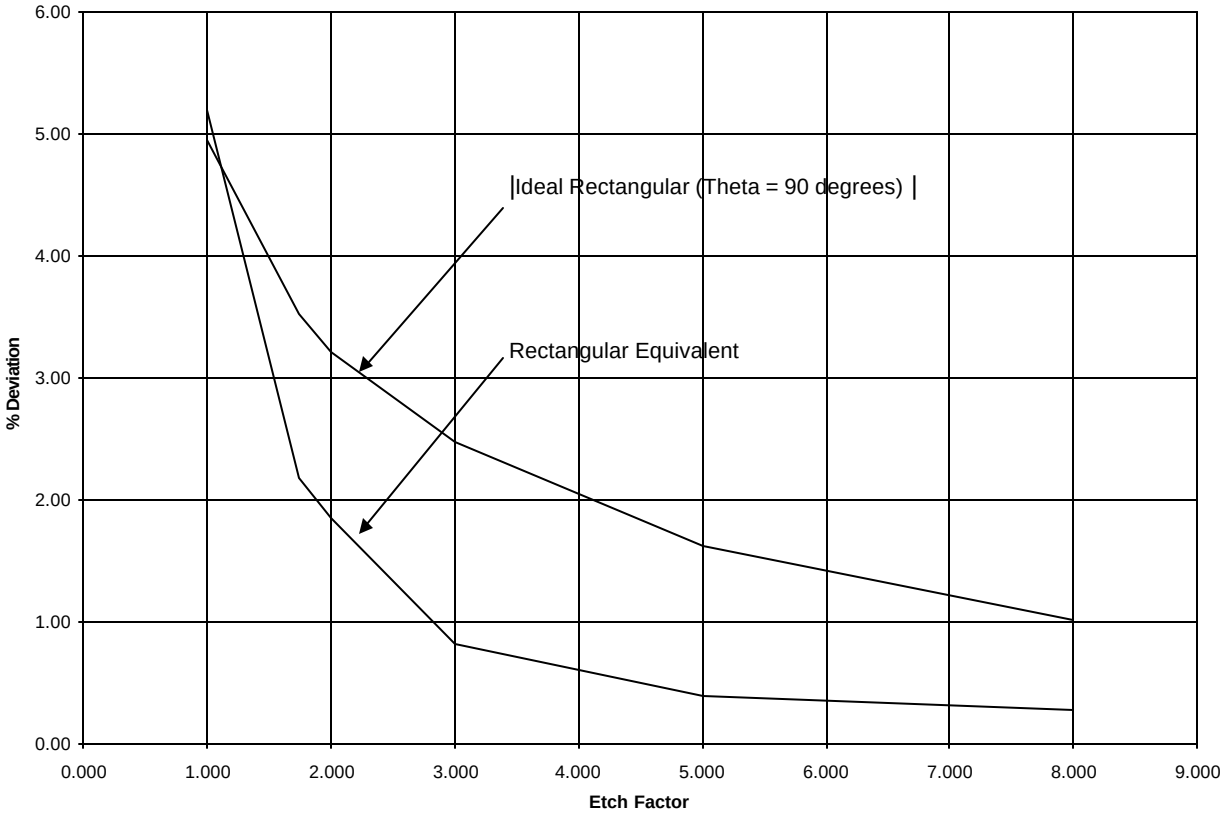


FIGURE 20: Characteristic Impedance Deviation With Respect to Actual Trapezoidal Cross Section; Edge-Coupled, Surface Microstrip

The broadside-coupled pair is another conductor configuration that finds application in differential signaling. This configuration is illustrated in Figure 21. The inverted version is *not recommended* as this implies that the conductors are on separate cores and thus subject to misalignment. Table 9 provides simulation data for the actual trapezoidal traces. Table 10 provides simulation data for the equivalent rectangular with the "%D (ER/AT)" column pertaining to the Table 9 trapezoidal values. The inverted trapezoidal data is presented in Table 11. Impedance deviation for the normal (not inverted) trapezoidal cross section is given in Figure 22.

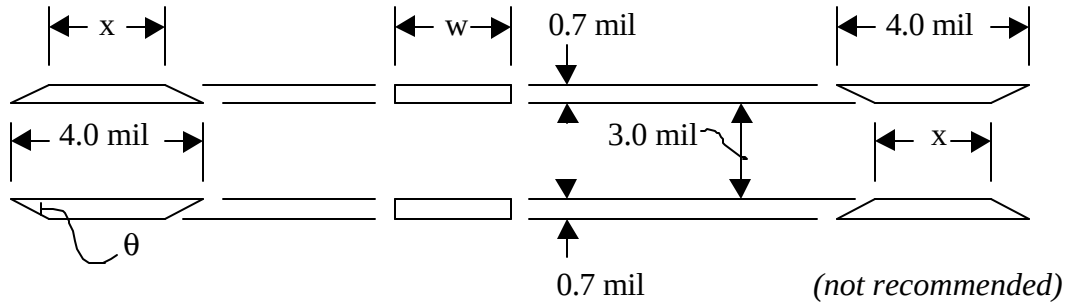


FIGURE 21: Broadside-Coupled Pair

TABLE 9: Broadside-Coupled Pair – Normal Configuration – Ideal Rectangular and Actual Trapezoidal

Etch Factor	Theta (deg)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (IR/AT)
Infinite	90.0	11.499	2.4971	67.859	*N/A*
1.000	45.0	12.306	2.3856	71.822	-5.51
1.732	60.0	11.877	2.4176	70.090	-3.18
2.000	63.4	11.822	2.4288	69.768	-2.74
3.000	71.6	11.732	2.4475	69.235	-1.99
5.000	78.7	11.646	2.4654	68.730	-1.27
8.000	82.9	11.590	2.4775	68.395	-0.78

TABLE 10: Broadside-Coupled Pair – Equivalent Rectangular – (%D referenced to Nomal Trapezoidal)

Etch Factor	w (mils)	L (nH/inch)	C (nH/inch)	Zo (Ohms)	%D (ER/AT)
1.000	3.30	12.724	2.2566	75.091	4.55
1.732	3.60	12.168	2.3597	71.810	2.45
2.000	3.65	12.078	2.3774	71.275	2.16
3.000	3.77	11.871	2.4187	70.058	1.18
5.000	3.86	11.726	2.4488	69.199	0.68
8.000	3.91	11.641	2.4665	68.701	0.45

TABLE 11: Broadside-Coupled Pair – Inverted (*not recommended)* Configuration

Etch Factor	x (mils)	L (nH/inch)	C (pF/inch)	Zo (Ohms)	%D (IR/AT)	%D (ER/AT)
1.000	2.60	12.636	2.2723	74.572	-9.00	0.70
1.732	3.19	12.221	2.3494	72.124	-5.91	-0.44
2.000	3.30	12.141	2.3749	71.499	-5.09	-0.31
3.000	3.53	11.949	2.4029	70.519	-3.77	-0.65
5.000	3.72	11.759	2.4417	69.398	-2.22	-0.29
8.000	3.83	11.667	2.4610	68.855	-1.45	-0.22

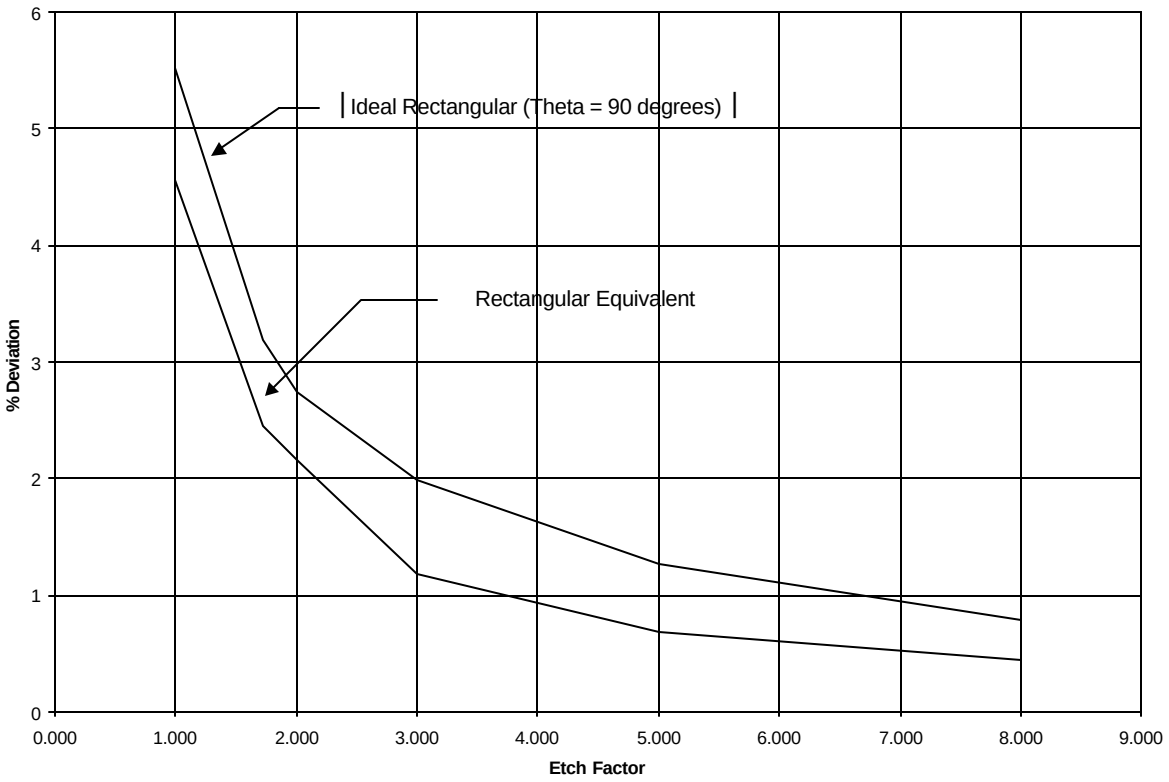


FIGURE 21: Characteristic Impedance Deviation With Respect to Actual Trapezoidal Cross Section; Broadside-Coupled Pair

Field Modeling Tools: Field modeling tools are essential for evaluating etch factor. Many of the available tools can only model rectangular cross sections. While the equivalent rectangular correction can improve results somewhat, it is not all that good for low etch factors. Many of the available tools have been designed for printed wiring boards with a ground return plane and are not capable of evaluating cables or the effects of shielding. Finding a tool that handles a floating shield is particularly troublesome.

We used *Ansoft* software to model the etch factor. This tool set can handle cables, non rectangular cross sections, and shielding effects. The Ansoft package is a suite of tools that includes the *Maxwell 2D field solver* that was used for our evaluation. The 2D tool requires that the transmission line section being analyzed have a uniform but not necessarily rectangular cross section. For non uniform structures Ansoft offers a 3D tool as well.

The Maxwell 2D solver uses geometry and material properties such as dielectric constant, resistivity, line width, line thickness, etceteras as inputs. Using finite element analysis Maxwell 2D provides electrical parameter outputs such as Z_0, C_{ij}, L_{ij}, etc. In addition, it can provide frequency sweeps such as L versus frequency and R versus frequency. Many of the board modeling tools provide only the high frequency solution.

The Ansoft tool has allowed us to establish design guidelines. It can provide absolute accuracy better than one percent. It allowed us to do a lot of quick "what if" evaluations. In general, this tool has allowed us to avoid expensive and time consuming cut and try hardware iterations.

As useful as the Ansoft tool is, it does have some drawbacks. The tool is not user friendly. It almost *always* provides an answer. The answer may not always be right. The user must be familiar enough with transmission line theory to detect gross inaccuracies. If these inaccuracies are found to exist parameters such as accuracy and meshing must be adjusted. It is useful to perform a frequency sweep of resistance. If R versus f levels off in the frequency range of interest, a finer mesh should be applied. The power and versatility of the tool has resulted in a rather complex arrangement that precludes casual use. There is a steep learning curve.

Conclusions:

Higher edge rates and clocks in digital logic force us to use transmission line analysis and impedance control.

Low etch factor increases impedance in excess of six percent for some configurations.

Etch factor varies from vendor to vendor due to different processes and equipment.

Etch factor can vary with the same vendor due to production at different plants or the refurbishing of old plants.

The rectangular correction factor is not all that good for low etch factors.

Appropriate field modeling tools are needed to fully evaluate etch factor.

References:

1] Johnson, Howard W. and Martin Graham, High-Speed Digital Design: A Handbook of Black Magic, PTR Prentice-Hall, 1993, ISBN 0-13-395724-1.

2] Buhler, ☺tto and Charles Grasso, "Transmission Line Inductance and Proximity Effect," 10th Annual IEEE EMC Society (Rocky Mountain Chapter) Regional Symposium, Tuesday, May 23, 2000 at the Holiday Inn, Denver Northglenn, 10 East 120th Avenue, Northglenn, Colorado.

3] Bogatin, Eric, "Impedance Calculations," November 1, 1999. Available as ID #73 from http://www.GigaTest.com

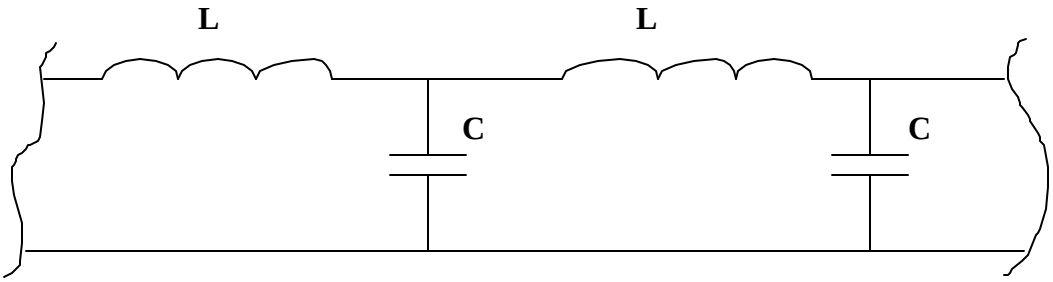
4] Printed Circuits Handbook, Coombs, Clyde F. Jr. ed., third edition, McGraw-Hill, 1988, ISBN 0-07-012609-7, pp 14.28 – 14.33.

6] Handbook of Flexible Circuits, Gilleo, Ken ed., Van Nostrand Reinhold, 1992, ISBN 0-442-00168-1, pp 45, 244.

Appendix (see next page)

TRANSMISSION LINE CRIB SHEET

Equivalent electrical circuit, Lossless Lumped Constant



L & C should be chosen such that T_{pd} per section < $(T_r)/6$, where T_r = rise time of signal

---

$Z_0 = \sqrt{L/C}$ **Z_0 = Characteristic impedance of transmission line in W.**

L = Transmission line inductance per unit length.

C = Transmission line capacitance per unit length.

$T_{pd} = \sqrt{LC}$ **T_{pd} = Transmission line signal delay per unit length.**

$v_p = c/\sqrt{\varepsilon_r}$ **v_p = Transmission line velocity of propagation.**

c = velocity of light in vacuum (299,792,458 m/s » 11.803 in/ns » 0.9836 ft/ns)

ε_r = relative dielectric constant of transmission line.

$T_{pd} = (T_{pd\text{-}vacuum})\sqrt{\varepsilon_r}$ **$T_{pd\text{-}vacuum}$ = 84.723 ps/inch**

$\varepsilon_r = (T_{pd}/T_{pd\text{-}vacuum})^2$

$\lambda f = c$ in vacuum **λ = wavelength**

$\lambda f = v_p$ in dielectric **f = frequency**

$C = T_{pd}/Z_0$

$L = Z_0 T_{pd}$

$$\rho = \frac{Z_L - Z_0}{Z_L + Z_0}$$

ρ = reflection coefficient (-1.0 to +1.0).

Z_L = Load impedance in Ω.

$$Z_L = \frac{Z_0(1 + \rho)}{(1 + \rho)}$$

A useful approximation for moderate mismatch

$\rho \approx$ (mismatch)/2

mismatch 20 % high	**mismatch 5 % high**
ρ = 9.09 % $\rho \approx$ 10 %	**ρ = 2.43 % $\rho \approx$ 2.5 %**
mismatch 20 % low	**mismatch 5 % low**
ρ = -11.11 % $\rho \approx$ -10 %	**ρ = -2.56 % $\rho \approx$ - 2.5 %**